

**Amendments to the Claims:** This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) An imaging system comprising:  
an array of pixel sensors;  
a first bank of sample-and-hold circuits connected to the pixel sensors;  
a second bank of sample-and-hold circuits connected to the pixel sensors;  
a first analog-to-digital converter;  
a second analog-to-digital converter; and  
a selection circuit operable to select and connect a sample-and-hold circuit from the first bank to the first analog-to-digital converter and simultaneously select and connect a sample-and-hold circuit from the second bank to the second analog-to-digital converter;  
wherein the sample-and-hold circuit from the first bank is selectively connected to a row of the array for sampling a succession of reset voltages only from corresponding columns of the selected row, and  
the sample-and-hold circuit from the second bank of the array is selectively connected to the same row of the array for sampling a succession of integrated voltages only from the corresponding columns of the same selected row;  
wherein the first and second banks of sample-and-hold circuits are directly connected to the pixel sensors, and  
the first and second analog-to-digital converters, respectively, are connected to the first and second banks of sample-and-hold circuits for independently digitizing the sampled succession of the reset and integrated voltages, respectively,  
a FIFO buffer is coupled to receive a digital output signal from the first analog-to-digital converter; and  
an adder is coupled to determine a difference between a digital output signal from the FIFO buffer and a digital output signal from the second analog-to-digital converter.
2. (Original) The system of claim 1, wherein the array includes a plurality of columns of the pixel sensors, and columns of pixel sensors are connected to respective sample-and-hold circuits in the first bank and to respective sample-and-hold circuits in the second bank.
3. (Canceled)

4. (Original) The system of claim 1, further comprising a control circuit that activates the first bank to sample reset voltages in a first selected set of pixel sensors and activates the second bank to sample integrated voltages in a second selected set of pixel sensors.

5. (Previously Presented) The system of claim 4, wherein the first selected set of pixel sensors consists of the pixel sensors that are in a row of the array that has just been reset.

6. (Original) The system of claim 4, wherein the first selected set of pixel sensors consists of the pixel sensors that are in a row of the array for which an exposure time has lapsed since a last reset of the row.

7. (Original) The system of claim 1, wherein:  
the selection circuit is operable in a digital correlated double sampling mode, wherein the selection circuit connects a selected sample-and-hold circuit from the first bank to the first analog-to-digital converter and simultaneously connects a selected sample-and-hold circuit from the second bank to the second analog-to-digital converter; and

the selection circuit is operable in an analog correlated double sampling mode, wherein the selection circuit simultaneously connects the selected sample-and-hold circuit from the first bank and the selected sample-and-hold circuit from the second bank to one of the first analog-to-digital converter and the second analog-to-digital converter.

8. (Currently Amended) An imaging method comprising:  
(a) resetting selected pixel sensors in an image sensor;  
(b) sampling and holding reset voltages of the selected pixel sensors;  
(c) converting the reset voltages to digital reset values using a first channel;  
(d) sampling and holding integrated voltage of the selected pixel sensors after lapse of an exposure time;  
(e) converting the integrated voltages to digital integrated values using a second channel;  
(f) changing which pixel sensors in the image sensor are the selected pixel sensors; and  
(g) repeating steps (a) to (f), wherein converting the integrated voltages overlaps with converting the reset voltage,

sampling and holding the reset voltages is performed by the first channel only and  
sampling and holding the integrated voltages is performed by the second channel only,

converting the reset and integrated voltages into digital reset and integrated values is performed after the sampling and holding of the reset and integrated voltages, respectively;

receiving in a FIFO buffer a digital output signal from the first channel; and  
determining a difference between the digital output signal from the FIFO buffer and a  
digital output signal from the second channel.

9. (Original) The method of claim 8, wherein converting the integrated voltages for pixel sensors overlaps with converting the reset voltage for other pixel sensors.

10. (Original) The method of claim 8, wherein converting the integrated voltages for pixel sensors that are capturing a first frame of a moving image overlaps with converting the reset voltage for other pixel sensors that are capturing a second frame of the moving image.

11. (Original) The method of claim 10, wherein repetitions of step (c) provide a continuous stream of the digital reset values including digital reset values for the first frame and the second frame.

12. (Original) The method of claim 10, wherein repetitions of step (e) provide a continuous stream of the digital integrated values including digital integrated values for the first frame and the second frame.

13. (Original) The method of claim 8, wherein repetitions of step (c) are separated by a time  $T_{out}$ , and each repetition of step (e) follows a corresponding repetition of step (c) by a time  $T_{exp}$ .

14. (Original) The method of claim 13, wherein the time  $T_{out}$  is about equal to a required time for output digital values corresponding to a row of the pixel sensors.

15. (Original) The method of claim 13, wherein the  $T_{exp}$  is about equal to an exposure time for an image.

16. (Original) The method of claim 8, wherein the first channel comprises a first analog-to-digital converter, and the second channel comprises a second analog-to-digital converter.

17. (Original) The method of claim 8, wherein repetitions of step (c) provide a continuous stream of the digital reset values.

18. (Original) The method of claim 8, wherein repetitions of step (e) provide a continuous stream of the digital integrated values.

19. (Previously Presented) The system of claim 1, wherein the succession of reset voltages and the succession of integrated voltages are configured for simultaneous sampling of the selected row by the sample-and-hold circuit from the first and second banks, respectively.